

**3V 8M-BIT
SERIAL NOR FLASH WITH
DUAL AND QUAD SPI**

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FEATURES

- **Low power supply operation**
 - Single 2.3V-3.6V supply
- **8M bit Serial Flash**
 - 8 M-bit/1,024K-byte/4,096 pages
 - 256 bytes per programmable page
 - Uniform 4K-byte Sectors, 32K/64K-byte Blocks
- **New Family of SpiFlash Memories**
 - Standard SPI: CLK, CS#, DI, DO, WP#, HOLD# / RESET#
 - Dual SPI: CLK, CS#, DI, DO, WP#, HOLD# / RESET#
 - Quad SPI: CLK, CS#, IO0, IO1, IO2, IO3
 - Software & Hardware Reset
 - Auto-increment Read capability
- **Temperature Ranges**
 - Industrial (-40°C to +85°C)
 - Extended (-20°C to +85°C)
- **Low power consumption**
 - 9 mA typical active current
 - 2 uA typical power down current
- **Efficient “Continuous Read” and Quad Read**
 - Continuous Read with 8/16/32/64-Byte Wrap
 - As few as 8 clocks to address memory
 - Quad Peripheral Interface reduces instruction overhead
- **Flexible Architecture with 4KB sectors**
 - Sector Erase (4K-bytes)
 - Block Erase (32K/64K-bytes)
 - Page Program up to 256 bytes
 - More than 100K erase/program cycles
 - More than 20-year data retention
- **Advanced Security Feature**
 - Software and Hardware Write-Protect
 - Power Supply Lock-Down and OTP protection
 - Top/Bottom, Complement array protection
 - 64-Bit Unique ID for each device
 - Discoverable parameters(SFDP) register
 - 3X256-Bytes Security Registers with OTP locks
 - Volatile & Non-volatile Status Register Bits
- **High performance program/erase speed**
 - Page program time: 400us typical
 - Sector erase time: 35ms typical
 - Block erase time: 200ms typical
 - Chip erase time: 10 Seconds typical
- **Package Options**
 - 8-pin SOIC 150/208-mil
 - 8-pad WSON 6x5-mm
 - 8-pin PDIP 300-mil
 - All Pb-free packages are RoHS compliant

GENERAL DESCRIPTION

The ZB25VQ80 of non-volatile flash memory device supports the standard Serial Peripheral Interface (SPI). Traditional SPI single bit serial input and output (Single I/O or SIO) is supported as well as optional two bit (Dual I/O or DIO) and four bit (quad I/O) serial protocols. This multiple width interface is called SPI Multi-I/O or MIO.

The SPI protocols use only 4 to 6 signals:

- ◆ Chip Select (CS#)
- ◆ Serial Clock (CLK)
- ◆ Serial Data
 - IO0 (DI)
 - IO1 (DO)
 - IO2 (WP#)
 - IO3 (HOLD# / RESET#)

The ZB25VQ80 support the standard Serial Peripheral Interface (SPI), Dual/Quad I/O SPI as well as 2-clocks instruction cycle Quad Peripheral Interface : Serial Clock, Chip Select, Serial Data I/O0 (DI), I/O1 (DO), I/O2 (WP#), and I/O3 (HOLD# / RESET#). SPI clock frequencies of up to 104MHz are supported allowing equivalent clock rates of 208MHz (104MHz x 2) for Dual I/O and 44MHz (104MHz x 4) for Quad I/O when using the Fast Read Dual/Quad I/O . These transfer rates can outperform standard Asynchronous 8 and 16-bit Parallel Flash memories. The Continuous Read Mode allows for efficient memory access with as few as 8-clocks of instruction-overhead to read a 24-bit address, allowing true XIP (execute in place) operation.

A Hold pin, Write Protect pin and programmable write protection, with top or bottom array control, provide further control flexibility. Additionally, the device supports JEDEC standard manufacturer and device ID and SFDP Register, a 64-bit Unique Serial Number and three 256-bytes Security Registers.

The ZB25VQ80 provides an ideal storage solution for systems with limited space, signal connections, and power. These memories' flexibility and performance is better than ordinary serial flash devices. They are ideal for code shadowing to RAM, executing code directly (XIP), and storing reprogrammable data.

1. ORDERING INFORMATION

The ordering part number is formed by a valid combination of the following:

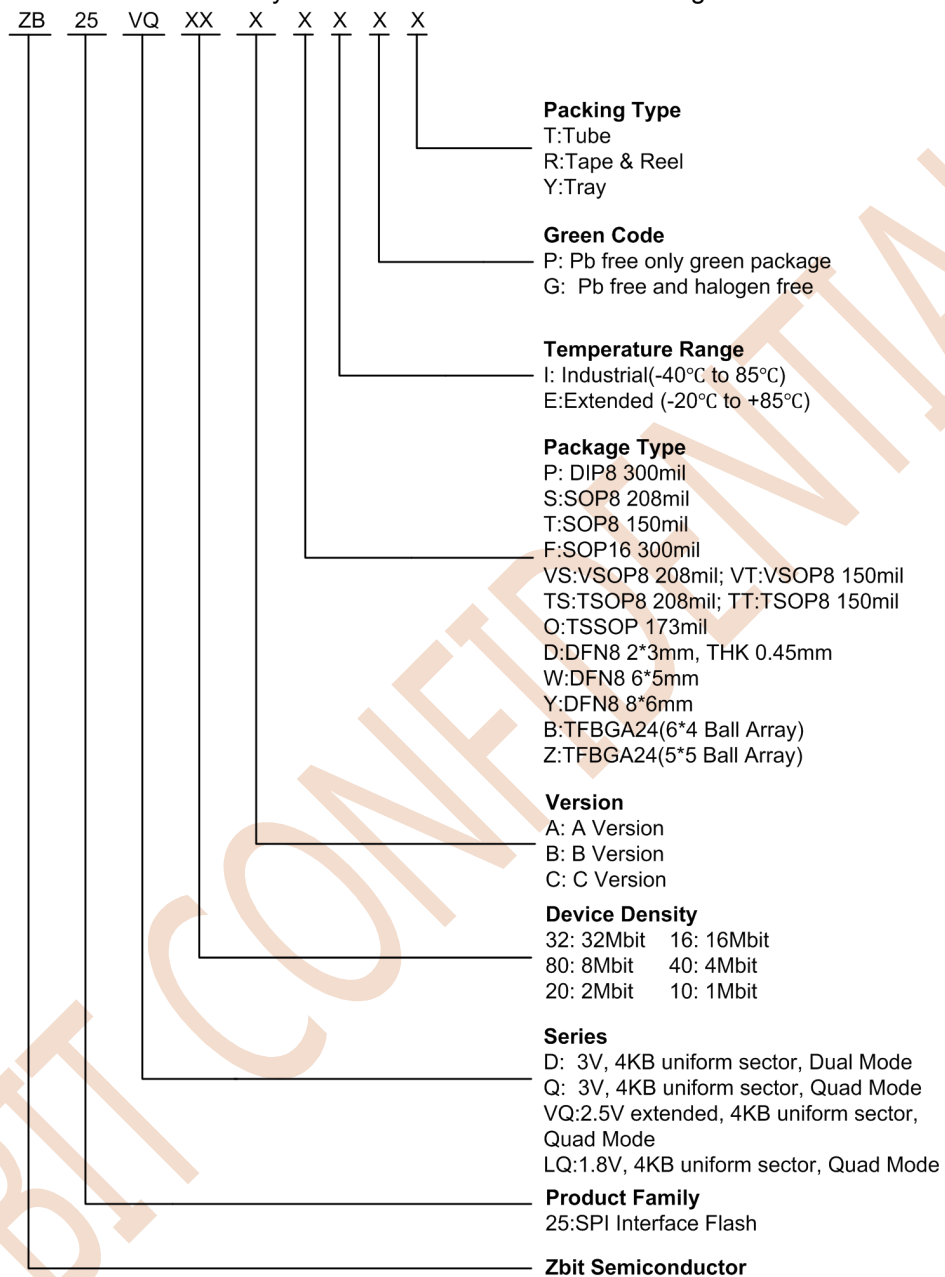


Figure 1.1 Ordering Information

2. BLOCK DIAGRAM

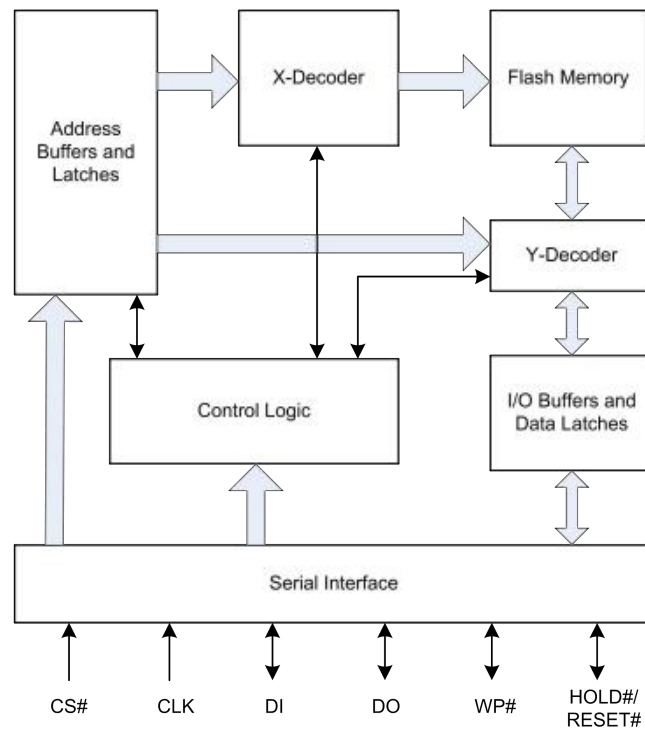


Figure 2.1 Block Diagram

3. CONNECTION DIAGRAMS

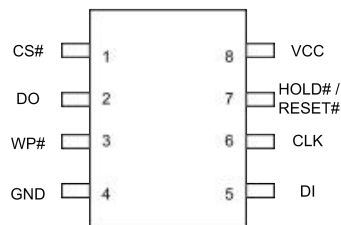


Figure 3.1 8-pin SOP (150/208mil)/ PDIP (300mil)

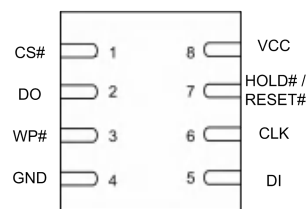


Figure 3.2 8-Contact 6 x 5 mm WSON

4. SIGNAL DESCRIPTIONS

Table 4.1 Pin Descriptions

Symbol	Pin Name
CLK	Serial Clock Input
DI(IO0)	Serial Data Input(Data input output 0) ⁽¹⁾
DO(IO1)	Serial Data Output(Data input output 1) ⁽¹⁾
CS#	Chip Enable
WP#(IO2) ⁽³⁾	Write Protect (Data input output 2) ⁽²⁾
HOLD# / RESET# ⁽³⁾ (IO3)	Hold or Reset input(Data input output 3) ⁽²⁾
V _{CC}	Power Supply (2.3-3.6V)
GND	Ground

Notes:

(1)IO0 and IO1 are used for Standard and Dual SPI instructions.

(2)IO0—IO3 are used for QUAD SPI instructions.

(3)WP# and HOLD# / RESET# functions are only available for Standard and Dual SPI.

4.1. Serial Data Input (DI) / IO0

The SPI Serial Data Input (DI) pin is used to transfer data serially into the device. It receives instructions, address and data to be programmed. Data is latched on the rising edge of the Serial Clock (CLK) input pin. The DI pin becomes IO0 - an input and output during Dual and Quad commands for receiving instructions, address, and data to be programmed (values latched on rising edge of serial CLK clock signal) as well as shifting out data (on the falling edge of CLK).

4.2. Serial Data Output (DO) / IO1

The SPI Serial Data Output (DO) pin is used to transfer data serially out of the device. Data is shifted out on the falling edge of the Serial Clock (CLK) input pin. DO becomes IO1 - an input and output during Dual and Quad commands for receiving instructions, addresses, and data to be programmed (values latched on rising edge of serial CLK clock signal) as well as shifting out data (on the falling edge of CLK).

4.3. Serial Clock (CLK)

The SPI Serial Clock Input (CLK) pin provides the timing for serial input and output operations. ("See SPI Mode")

4.4. Chip Select (CS#)

The SPI Chip Select (CS#) pin enables and disables device operation. When CS# is high the device is deselected and the Serial Data Output pins are at high impedance.

When deselected, the devices power consumption will be at standby levels unless an internal erase, program or status register cycle is in progress. When CS# is brought low the device will be selected, power consumption will increase to active levels and instructions can be written to and data read from the device. After power-up, CS# must transition from high to low before a new instruction will be accepted.

4.5. Write Protect (WP#) / IO2

The Write Protect (WP#) pin can be used to prevent the Status Register from being written. Used in conjunction with the Status Register's Block Protect (BP0, BP1 and BP2, TB, SEC, CMP) bits and Status Register Protect (SRP0) bits, a portion or the entire memory array can be hardware protected.

The WP# function is not available when the Quad mode is enabled. The WP# function is replaced by IO2 for input and output during Quad mode for receiving addresses and data to be programmed (values are latched on rising edge of the CLK signal) as well as shifting out data (on the falling edge of CLK).

4.6. HOLD (HOLD#) / IO3

The HOLD# pin allows the device to be paused while it is actively selected. When HRSW bit is '0' (factory default is '0'), the HOLD# pin is enabled. When HOLD# is brought low, while CS# is low, the DO pin will be at high impedance and signals on the DI and CLK pins will be ignored (don't care). When HOLD# is brought high, device operation can resume. The HOLD# function can be useful when multiple devices are sharing the same SPI signals. The HOLD# pin is active low. When the QE bit of Status Register-2 is set for Quad I/O, the HOLD# pin function is not available since this pin is used for IO3.

4.7. RESET (RESET#) / IO3

The RESET# pin allows the device to be reset by the controller. When HRSW bit is '1' (factory default is '0'), the RESET# pin is enabled. Drive RESET# low for a minimum period of ~1us (tRESET*) will interrupt any on-going external/internal operations, regardless the status of other SPI signals (CS#, CLK, DI, DO, WP# and/or HOLD#). The Hardware Reset function is only available for standard SPI and Dual SPI operation, when QE=0, the IO3 pin can be configured either as a HOLD# pin or as a RESET# pin depending on Status Register setting, when QE=1, this pin is the Serial Data IO (IO3) for Quad I/O operation.

5. MEMORY ORGANIZATION

5.1. Flash Memory Array

The ZB25VQ80 memory is organized as:

- 1,048,576bytes
- Uniform Sector Architecture 16 blocks of 64-Kbyte
- 256 sectors of 4-Kbyte
- 4, 096 pages (256 bytes each)

Each page can be individually programmed (bits are programmed from 1 to 0). The device is Sector, Block or Chip Erasable but not Page Erasable.

Table 5.1⁽¹⁾ Memory Organization(ZB25VQ80)

Block/ Security Register/SFDP	Sector	Address range	
Security Register 3	-	003000H	0030FFH
Security Register 2	-	002000H	0020FFH
Security Register 1	-	001000H	0010FFH
Security Register 0 (SFDP)	-	000000H	0000FFH
Block 15	255	0FF000H	0FFFFFFH

	240	0F0000H	0F0FFFH
Block 14	239	0EF000H	0EFFFFFFH

	224	0E0000H	0E0FFFH
.....

.....

Block 2	47	02F000H	02FFFFFFH

	32	020000H	020FFFH
Block 1	31	01F000H	01FFFFFFH

	16	010000H	010FFFH
Block 0	15	00F000H	00FFFFFFH

	0	000000H	000FFFH

Notes:

(1) These are condensed tables that use a couple of sectors as references. There are address ranges that are not explicitly listed. All 4-kB sectors have the pattern XXX000h-XXXXFFh.

5.2. Security Registers

The ZB25VQ80 provides four 256-byte Security Registers. Each register can be used to store information that can be permanently protected by programming One Time Programmable (OTP) lock bits in Status Register-2.

Register 0 is used by ZBIT to store and protect the Serial Flash Discoverable Parameters (SFDP) information that is also accessed by the Read SFDP command. See Table 5.1.

The three additional Security Registers can be erased, programmed, and protected individually. These registers may be used by system manufacturers to store and permanently protect security or other important information separate from the main memory array.

5.2.1 Security Register 0

Serial Flash Discoverable Parameters (SFDP — JEDEC JESD216B):

This document defines the Serial Flash Discoverable Parameters (SFDP) revision B data structure for ZB25VQ80 family.

The Read SFDP (RSFDP) command (5Ah) reads information from a separate flash memory address space for device identification, feature, and configuration information, in accord with the JEDEC JESD216B standard for Serial Flash Discoverable Parameters.

The SFDP data structure consists of a header table that identifies the revision of the JESD216 header format that is supported and provides a revision number and pointer for each of the SFDP parameter tables that are provided. The parameter tables follow the SFDP header. However, the parameter tables may be placed in any physical location and order within the SFDP address space. The tables are not necessarily adjacent nor in the same order as their header table entries.

The SFDP header points to the following parameter tables:

- Basic Flash
 - This is the original SFDP table.

The physical order of the tables in the SFDP address space is: SFDP Header, and Basic Flash. The SFDP address space is programmed by ZBIT and read-only for the host system.

5.2.2 Serial Flash Discoverable Parameters (SFDP) Address Map

The SFDP address space has a header starting at address zero that identifies the SFDP data structure and provides a pointer to each parameter. One Basic Flash parameter is mandated by the JEDEC JESD216B standard.

Table 5.2 SFDP Overview Map — Security Register 0

Byte Address	Description
0000h	Location zero within JEDEC JESD216B SFDP space – start of SFDP header
0010h	Undefined space reserved for future SFDP header
0030h	Start of SFDP parameter
...	Remainder of SFDP JEDEC parameter followed by undefined space
006Fh	End of SFDP space
0070h to 00FFh	Reserved space

5.2.3 SFDP Header Field Definitions

Table 5.3 SFDP Header

SFDP Byte Address	SFDP Dword Name	Data	Description
00h	SFDP Header 1st DWORD	53h	This is the entry point for Read SFDP (5Ah) command i.e. location zero within SFDP space ASCII "S"
01h		46h	ASCII "F"
02h		44h	ASCII "D"
03h		50h	ASCII "P"
04h	SFDP Header 2nd DWORD	06h	SFDP Minor Revision (06h = JEDEC JESD216 Revision B) – This revision is backward compatible with all prior minor revisions. Minor revisions are changes that define previously reserved fields, add fields to the end, or that clarify definitions of existing fields. Increments of the minor revision value indicate that previously reserved parameter fields may have been assigned a new definition or entire Dwords may have been added to the parameter table. However, the definition of previously existing fields is unchanged and therefore remains backward compatible with earlier SFDP parameter table revisions. Software can safely ignore increments of the minor revision number, as long as only those parameters the software was designed to support are used i.e. Previously reserved fields and additional Dwords must be masked or ignored. Do not do a simple compare on the minor revision number, looking only for a match with the revision number that the software is designed to handle. There is no problem with using a higher number minor revision.
05h		01h	SFDP Major Revision – This is the original major revision. This major revision is compatible with all SFDP reading and parsing software.
06h		00h	Number of Parameter Headers (zero based, 00h = 1 parameters)
07h		FFh	Unused
08h	Parameter Header 0 1st DWORD	00h	Parameter ID LSB (00h = JEDEC SFDP Basic SPI Flash Parameter)
09h		06h	Parameter Minor Revision (00h = JESD216) –This older revision parameter header is provided for any legacy SFDP reading and parsing software that requires seeing a minor revision 6 parameter header. SFDP software designed to handle later minor revisions should continue reading parameter headers looking for a higher numbered minor revision that contains additional parameters for that software revision.
0Ah		01h	Parameter Major Revision (01h = The original major revision - all SFDP software is compatible with this major revision).
0Bh		10h	Parameter Table Length (in double words = Dwords = 4-byte units) 10h = 16 Dwords
0Ch	Parameter Header 0 2nd DWORD	30h	Parameter Table Pointer Byte 0 (Dword = 4-byte aligned) JEDEC Basic SPI Flash parameter byte offset = 30h
0Dh		00h	Parameter Table Pointer Byte 1
0Eh		00h	Parameter Table Pointer Byte 2
0Fh		FFh	Parameter ID MSB (FFh = JEDEC defined legacy Parameter ID)

5.2.4 JEDEC SFDP Basic SPI Flash Parameter

Table 5.4 Basic SPI Flash Parameter, JEDEC SFDP Rev B (Sheet 1 of 5)

SFDP Parameter Relative Byte Address	SFDP Dword Name	Data	Description
30h	JEDEC Basic Flash Parameter Dword-1	E5h	Start of SFDP JEDEC parameter Bits 7:5 = unused = 111b Bit 4:3 = 05h is volatile status register write instruction and status register is default non-volatile= 00b Bit 2 = Program Buffer > 64 bytes = 1 Bits 1:0 = Uniform 4-kB erase is supported throughout the device = 01b
31h		20h	Bits 15:8 = Uniform 4-kB erase instruction = 20h
32h		F1h	Bit 23 = Unused = 1b Bit 22 = Supports QOR Read (1-1-4), Yes = 1b Bit 21 = Supports QIO Read (1-4-4), Yes = 1b Bit 20 = Supports DIO Read (1-2-2), Yes = 1b Bit 19 = Supports DDR, No = 0 b Bit 18:17 = Number of Address Bytes 3 only = 00b Bit 16 = Supports SIO and DIO Yes = 1b Binary Field: 1-1-1-1-0-00-1 Nibble Format: 1111_0001 Hex Format: F1
33h		FFh	Bits 31:24 = Unused = FFh
34h	JEDEC Basic Flash Parameter Dword-2	FFh	Density in bits, zero based, 2 Mb = 001FFFFFFh 4 Mb = 003FFFFFFh 8 Mb = 007FFFFFFh
35h		FFh	
36h		7Fh	
37h		00h	
38h	JEDEC Basic Flash Parameter Dword-3	44h	Bits 7:5 = number of QIO (1-4-4) Mode cycles = 010b Bits 4:0 = number of Fast Read QIO Dummy cycles = 00100b for default latency code
39h		EBh	Fast Read QIO (1-4-4) instruction code
3Ah		08h	Bits 23:21 = number of Quad Out (1-1-4) Mode cycles = 000b Bits 20:16 = number of Quad Out Dummy cycles = 01000b for default latency code
3Bh		6Bh	Quad Out (1-1-4) instruction code
3Ch	JEDEC Basic Flash Parameter Dword-4	08h	Bits 7:5 = number of Dual Out (1-1-2) Mode cycles = 000b Bits 4:0 = number of Dual Out Dummy cycles = 01000b for default latency code
3Dh		3Bh	Dual Out (1-1-2) instruction code
3Eh		80h	Bits 23:21 = number of Dual I/O Mode cycles = 100b Bits 20:16 = number of Dual I/O Dummy cycles = 00000b for default latency code
3Fh		BBh	Dual I/O instruction code
40h	JEDEC Basic Flash Parameter Dword-5	FFh	Bits 7:5 RFU = 111b Bit 4 = QPI (4-4-4) fast read commands not supported = 0b Bits 3:1 RFU = 111b Bit 0 = Dual All not supported = 0b
41h		FFh	Bits 15:8 = RFU = FFh
42h		FFh	Bits 23:16 = RFU = FFh
43h		FFh	Bits 31:24 = RFU = FFh
44h	JEDEC Basic Flash Parameter Dword-6	FFh	Bits 7:0 = RFU = FFh
45h		FFh	Bits 15:8 = RFU = FFh
46h		FFh	Bits 23:21 = number of Dual All Mode cycles = 111b Bits 20:16 = number of Dual All Dummy cycles = 11111b
47h		FFh	Dual All instruction code

Table 5.4 Basic SPI Flash Parameter, JEDEC SFDP Rev B (Sheet 2 of 5)

SFDP Parameter Relative Byte Address	SFDP Dword Name	Data	Description
48h	JEDEC	0Ch	Erase Type 1 size 2^N Bytes = 4 kB = 0Ch (for Uniform 4 kB)
49h	Basic Flash Parameter	20h	Erase Type 1 instruction
4Ah		0Fh	Erase Type 2 size 2^N Bytes = 32 kB = 0Fh (for Uniform 32 kB)
4Bh	Dword-8	52h	Erase Type 2 instruction
4Ch	JEDEC	10h	Erase Type 3 size 2^N Bytes = 64 kB = 10h (for Uniform 64 kB)
4Dh	Basic Flash Parameter	D8h	Erase Type 3 instruction
4Eh		00h	Erase Type 4 size 2^N Bytes = not supported = 00h
4Fh	Dword-9	FFh	Erase Type 4 instruction = not supported = FFh
50h	JEDEC Basic Flash Parameter Dword-4	13h	Bits 31:30 = Erase Type 4 Erase, Typical time units (00b: 1 ms, 01b: 16 ms, 10b: 128 ms, 11b:1 s) = RFU = 11b Bits 29:25 = Erase Type 4 Erase, Typical time count = RFU = 11111b (typ erase time = (count+1) * units) = RFU = 11111
51h		42h	Bits 24:23 = Erase Type 3 Erase, Typical time units (00b: 1 ms, 01b: 16 ms, 10b: 128 ms, 11b:1 s) = RFU = 01b
52h		ADh	Bits 22:18 = Erase Type 3 Erase, Typical time count = 01011b (typ erase time = (count + 1) * units) = 12×16 ms = 200ms Bits 17:16 = Erase Type 2 Erase, Typical time units (00b: 1 ms, 01b: 16 ms, 10b: 128 ms, 11b:1 s) = 16 ms = 01b Bits 15:11 = Erase Type 2 Erase, Typical time count = 01000b (typ erase time = (count + 1) * units) = 9×16 ms = 150 ms Bits 10:9 = Erase Type 1 Erase, Typical time units (00b: 1 ms, 01b: 16 ms, 10b: 128 ms, 11b: 1s) = 16ms = 01b Bits 8:4 = Erase Type 1 Erase, Typical time count = 00001b (typ erase time = (count + 1) * units) = 2×16 ms = 35 ms Bits 3:0 = Count = (Max Erase time / (2 * Typical Erase time)) - 1 = 0011b Multiplier from typical erase time to maximum erase time = 8x multiplier Max Erase time = $2 \times (\text{Count} + 1) \times \text{Typ Erase time}$ Binary Fields: 1111111_0101011_0101000_0100001_0011 Nibble Format: 1111_1110_1010_1101_0100_0010_0001_0011 Hex Format: FE_AD_42_13
53h		FEh	



Table 5.4 Basic SPI Flash Parameter, JEDEC SFDP Rev B (Sheet 3 of 5)

SFDP Parameter Relative Byte Address	SFDP Dword Name	Data	Description
54h	JEDEC Basic Flash Parameter Dword-11	81h	Bits 23 = Byte Program Typical time, additional byte units (0b:1 μ s, 1b:8 μ s) = 1 μ s = 0b
55h		65h	Bits 22:19 = Byte Program Typical time, additional byte count, (count+1)*units, count = 0010b, (typ Program time = (count +1) * units) = 3*1 μ s = 3 μ s Bits 18 = Byte Program Typical time, first byte units (0b:1 μ s, 1b:8 μ s) = 8 μ s = 1b Bits 17:14 = Byte Program Typical time, first byte count, (count+1)*units, count = 0001b, (typ Program time = (count +1) * units) = 2*8 μ s = 16 μ s Bits 13 = Page Program Typical time units (0b:8 μ s, 1b:64 μ s) = 64 μ s = 1b Bits 12:8 = Page Program Typical time count, (count+1)*units, count = 00101b, (typ Program time = (count +1) * units) = 6*64 μ s = 400 μ s Bits 7:4 = N = 1000b, Page size= 2N = 256B page Bits 3:0 = Count = 0001b = (Max Page Program time / (2 * Typ Page Program time))- 1 Multiplier from typical Page Program time to maximum Page Program time = 4x multiplier Max Page Program time = 2*(Count +1)*Typ Page Program time Binary Fields: 0-0010-1-0001-1-00101-1000-0001 Nibble Format: 0001_0100_0110_0101_1000_0001 Hex Format: 14_65_81
56h		14h	8 Mb = 1010_1011b = ABh Bit 31 Reserved = 1b Bits 30:29 = Chip Erase, Typical time units (00b: 16 ms, 01b: 256 ms, 10b: 4 s, 11b: 64 s) = 256ms= 01b Bits 28:24 = Chip Erase, Typical time count, (count+1)*units, count = 01101b, (typ Program time = (count +1) * units) = 12*256ms = 3s
57h		ABh	
58h	JEDEC Basic Flash Parameter Dword-12	EDh	Bit 31 = Suspend and Resume supported = 0b
59h		63h	Bits 30:29 = Suspend in-progress erase max latency units (00b: 128ns, 01b: 1 μ s, 10b: 8 μ s, 11b: 64 μ s) = 1 μ s= 01b
5Ah		16h	Bits 28:24 = Suspend in-progress erase max latency count = 10011b, max erase suspend latency = (count +1) * units = 20*1 μ s = 20 μ s Bits 23:20 = Erase resume to suspend interval count = 0001b, interval = (count +1) * 64 μ s = 2* 64 μ s = 128 μ s Bits 19:18 = Suspend in-progress program max latency units (00b: 128ns, 01b: 1 μ s, 10b: 8 μ s, 11b: 64 μ s) = 1 μ s= 01b Bits 17:13 = Suspend in-progress program max latency count = 10011b, max erase suspend latency = (count +1) * units = 20*1 μ s = 20 μ s Bits 12:9 = Program resume to suspend interval count = 0001b, interval = (count +1) * 64 μ s = 2 * 64 μ s = 128 μ s Bit 8 = RFU = 1b Bits 7:4 = Prohibited operations during erase suspend = xxx0b: May not initiate a new erase anywhere (erase nesting not permitted) + xx1xb: May not initiate a page program in the erase suspended sector size + x1xxb: May not initiate a read in the erase suspended sector size + 1xxxb: The erase and program restrictions in bits 5:4 are sufficient = 1110b Bits 3:0 = Prohibited Operations During Program Suspend = xxx1b: May not initiate a new erase in the program suspended page size + xx0xb: May not initiate a new page program anywhere (program nesting not permitted) + x1xxb: May not initiate a read in the program suspended page size + 1xxxb: The erase and program restrictions in bits 1:0 are sufficient = 1101b Binary Fields: 0-01-10011-0001-01-10011-0001-1-1110-1101 Nibble Format: 0011_0011_0001_0110_0110_0011_1110_1101 Hex Format: 33_16_63_ED
5Bh		33h	

Table 5.4 Basic SPI Flash Parameter, JEDEC SFDP Rev B (Sheet 4 of 5)

SFDP Parameter Relative Byte Address	SFDP Dword Name	Data	Description
5Ch	JEDEC Basic Flash Parameter Dword-13	7Ah	Bits 31:24 = Erase Suspend Instruction = 75h Bits 23:16 = Erase Resume Instruction = 7Ah Bits 15:8 = Program Suspend Instruction = 75h Bits 7:0 = Program Resume Instruction = 7Ah
5Dh		75h	
5Eh		7Ah	
5Fh		75h	
60h	JEDEC Basic Flash Parameter Dword-14	F7h	Bit 31 = Deep Power-Down Supported = 0 Bits 30:23 = Enter Deep Power-Down Instruction = B9h Bits 22:15 = Exit Deep Power-Down Instruction = ABh Bits 14:13 = Exit Deep Power-Down to next operation delay units = (00b: 128 ns, 01b: 1 μ s, 10b: 8 μ s, 11b: 64 μ s) = 1 μ s = 01b Bits 12:8 = Exit Deep Power-Down to next operation delay count = 00010b, Exit Deep Power-Down to next operation delay = (count+1)*units = 3*1 μ s=3 μ s Bits 7:4 = RFU = 1111b Bit 3:2 = Status Register Polling Device Busy = 01b: Legacy status polling supported = Use legacy polling by reading the Status Register with 05h instruction and checking WIP bit[0] (0=ready; 1=busy). Bits 1:0 = RFU = 11b Binary Fields: 0-10111001-10101011-01-00010-1111-01-11 Nibble Format: 0101_1100_1101_0101_1010_0010_1111_0111 Hex Format: 5C_D5_A2_F7
61h		A2h	
62h		D5h	
63h		5Ch	
64h	JEDEC Basic Flash Parameter Dword-15	19h	Bits 31:24 = RFU = FFh Bit 23 = Hold and WP Disable = set QE(bit 1 of SR2) high = 1b Bits 22:20 = Quad Enable Requirements = 101b: QE is bit 1 of the status register 2. Status register 1 is read using Read Status instruction 05h. Status register 2 is read using instruction 35h. QE is set via Write Status instruction 01h with two data bytes where bit 1 of the second byte is one. It is cleared via Write Status with two data bytes where bit 1 of the second byte is zero. Bits 19:16 0-4-4 Mode Entry Method = xxx1b: Mode Bits[7:0] = A5h Note: QE must be set prior to using this mode + x1xxb: Mode Bits[7:0] = Axh + 1xxb: RFU = 1101b Bits 15:10 0-4-4 Mode Exit Method = xx_1xxb: Mode Bits[7:0] = 00h will terminate this mode at the end of the current read operation + xx_1xxb: Input Fh (mode bit reset) on DQ0-DQ3 for 8 clocks. This will terminate the mode prior to the next read operation. + 11_x1xx: RFU = 111101b Bit 9 = 0-4-4 mode supported = 1 Bits 8:4 = 4-4-4 mode enable sequences = 0_0001b: set QE per QER description above, then issue instruction 38h Bits 3:0 = 4-4-4 mode disable sequences = xxx1b: issue FFh instruction + 1xxb: issue the Soft Reset 66/99 sequence = 1001b Binary Fields: 11111111-1-101-1101-111101-1-00001-1001 Nibble Format: 1111_1111-1101-1101-1111_0110_0001-1001 Hex Format: FF_DD_F6_19
65h		F6h	
66h		DDh	
67h		FFh	

Table 5.4 Basic SPI Flash Parameter, JEDEC SFDP Rev B (Sheet 5 of 5)

SFDP Parameter Relative Byte Address	SFDP Dword Name	Data	Description
68h	JEDEC Basic Flash Parameter Dword-16	E8h	Bits 31:24 = Enter 4-Byte Addressing = xxxx_xxx1b:issue instruction B7 (preceding write enable not required) + xx1x_xxxx: Supports dedicated 4-byte address instruction set. Consult vendor data sheet for the instruction set definition or look for 4-byte Address Parameter Table. + 1xxx_xxxx: Reserved = 10000000b not supported Bits 23:14 = Exit 4-byte Addressing = xx_xxxx_xxx1b:issue instruction E9h to exit 4-byte address mode (Write enable instruction 06h is not required) + xx_xx1x_xxxx: Hardware reset + xx_x1xx_xxxx: Software reset (see bits 13:8 in this DWORD) + xx_1xxx_xxxx: Power cycle + x1_xxxx_xxxx: Reserved + 1x_xxxx_xxxx: Reserved = 11_0000_0000b not supported Bits 13:8 = Soft Reset and Rescue Sequence Support = x1_xxxx: issue reset enable instruction 66h, then issue reset instruction 99h. The reset enable, reset sequence may be issued on 1,2, or 4 wires depending on the device operating mode + 1x_xxxx: exit 0-4-4 mode is required prior to other reset sequences above if the device may be operating in this mode. = 11_0000b Bit 7 = RFU = 1 Bits 6:0 = Volatile or Non-Volatile Register and Write Enable Instruction for Status Register 1 = xxx_1xxx: Non-Volatile/Volatile status register 1 powers-up to last written value in the nonvolatile status register, use instruction 06h to enable write to non-volatile status register. Volatile status register may be activated after power-up to override the non-volatile status register, use instruction 50h to enable write and activate the volatile status register. + x1x_xxxx: Reserved + 1xx_xxxx: Reserved = 1101000b Binary Fields: 10000000-1100000000-110000-1-1101000 Nibble Format: 1000_0000_1100_0000_0011_0000_1110_1000 Hex Format: 80_C0_30_E8
69h		30h	
6Ah		C0h	
6Bh		80h	

6. FUNCTION DESCRIPTION

6.1 SPI Operations

6.1.1 SPI Modes

The ZB25VQ80 can be driven by an embedded microcontroller (bus master) in either of the two following clocking modes.

◆ **Mode 0** with Clock Polarity (CPOL) = 0 and, Clock Phase (CPHA) = 0

◆ **Mode 3** with CPOL = 1 and, CPHA = 1

For these two modes, input data is always latched in on the rising edge of the CLK signal and the output data is always available on the falling edge of the CLK clock signal.

The difference between the two modes is the clock polarity when the bus master is in standby mode and not transferring any data.

◆ CLK will stay at logic low state with CPOL = 0, CPHA = 0

◆ CLK will stay at logic high state with CPOL = 1, CPHA = 1

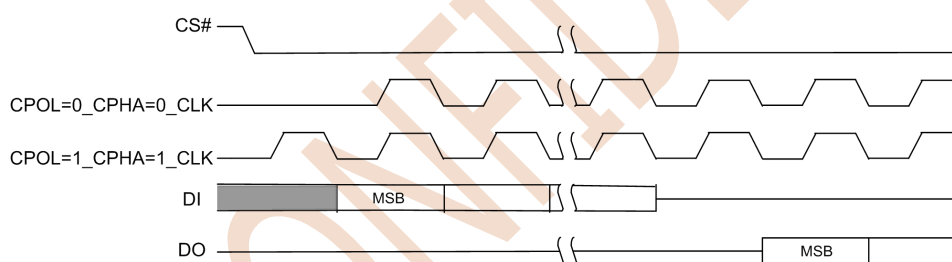


Figure 6.1 SPI Modes

Timing diagrams throughout the rest of the document are generally shown as both mode 0 and 3 by showing CLK as both high and low at the fall of CS#. In some cases a timing diagram may show only mode 0 with CLK low at the fall of CS#. In such case, mode 3 timing simply means clock is high at the fall of CS# so no CLK rising edge set up or hold time to the falling edge of CS# is needed for mode 3.

CLK cycles are measured (counted) from one falling edge of CLK to the next falling edge of CLK. In mode 0 the beginning of the first CLK cycle in a command is measured from the falling edge of CS# to the first falling edge of CLK because CLK is already low at the beginning of a command.

6.1.2 Dual SPI Modes

The ZB25VQ80 supports Dual SPI Operation when using the Fast Read Dual Output (3Bh) and Fast Dual I/O (BBh) instruction. These features allow data to be transferred from the device at twice the rate possible with the standard SPI. These instructions are ideal for quickly downloading code to RAM upon Power-up (code-shadowing) or for executing non-speed-critical code directly from the SPI bus (XIP). When using Dual SPI commands, the DI and DO pins become bidirectional I/O pins: IO0 and IO1.

6.1.3 Quad SPI Modes

The ZB25VQ80 supports Quad SPI operation when using the Fast Read Quad Output (6Bh), Fast Read Quad I/O (EBh) instruction, Word Read Quad I/O (E7h), and Octal Word Read Quad I/O (E3h). These instructions allow data to be transferred to or from the device four times the rate of ordinary Serial Flash. The Quad Read instructions offer a significant improvement in continuous and random access transfer rates

allowing fast code-shadowing to RAM or execution directly from the SPI bus (XIP). When using Quad SPI instructions, the DI and DO pins become bidirectional IO0 and IO1, and the WP# and HOLD# / RESET# pins become IO2 and IO3 respectively. Quad SPI instructions require the non-volatile Quad Enable bit (QE) in Status Register-2 to be set.

6.1.4 Hold Function

For Standard SPI and Dual SPI operations, the HOLD# / RESET# (IO3) signal allows the device interface operation to be paused while it is actively selected (when CS# is low). The Hold function may be useful in cases where the SPI data and clock signals are shared with other devices. For example, if the page buffer is only partially written when a priority interrupt requires use of the SPI bus, the Hold function can save the state of the interface and the data in the buffer so programming command can resume where it left off once the bus is available again. The Hold function is only available for standard SPI and Dual SPI operation, not during Quad SPI.

To initiate a Hold condition, the device must be selected with CS# low. A Hold condition will activate on the falling edge of the HOLD# signal if the CLK signal is already low. If the CLK is not already low the Hold condition will activate after the next falling edge of CLK. The Hold condition will terminate on the rising edge of the HOLD# signal if the CLK signal is already low. If the CLK is not already low the Hold condition will terminate after the next falling edge of CLK. During a Hold condition, the Serial Data Output, (DO) or IO0 and IO1, are high impedance and Serial Data Input, (DI) or IO0 and IO1, and Serial Clock (CLK) are ignored. The Chip Select (CS#) signal should be kept active (low) for the full duration of the Hold operation to avoid resetting the internal logic state of the device.

6.1.5 Software Reset & Hardware RESET# pin

The ZB25VQ80 can be reset to the initial power-on state by a software Reset sequence, either in SPI mode. This sequence must include two consecutive commands: Enable Reset (66h) & Reset (99h). If the command sequence is successfully accepted, the device will take approximately 10 μ s (t_{RST}) to reset. No command will be accepted during the reset period.

ZB25VQ80 can also be configured to utilize a hardware RESET# pin. The HRSW bit in the Status Register-3 is the configuration bit for HOLD# pin function or RESET# pin function. When HRSW=0 (factory default), the pin acts as a HOLD# pin as described above; when HRSW =1, the pin acts as a RESET# pin. Drive the RESET# pin low for a minimum period of \sim 1 μ s (t_{RESET}^*) will reset the device to its initial power-on state. Any on-going Program/Erase operation will be interrupted and data corruption may happen. While RESET# is low, the device will not accept any command input.

If QE bit is set to 1, the HOLD# or RESET# function will be disabled, the pin will become one of the four data I/O pins.

Hardware RESET# pin has the highest priority among all the input signals. Drive RESET# low for a minimum period of \sim 1 μ s (t_{RESET}^*) will interrupt any on-going external/internal operations, regardless the status of other SPI signals (CS#, CLK, DI, DO, WP# and/or HOLD#).

Note:

1. While a faster RESET# pulse (as short as a few hundred nanoseconds) will often reset the device, a 1 μ s minimum is recommended to ensure reliable operation.

6.2. Status Register

The Read and Write Status Registers commands can be used to provide status and control of the flash memory device.

Status Register-1 (SR1) and Status Register-2 (SR2) can be used to provide status on the availability of the flash memory array, whether the device is write enabled or disabled, the state of write protection, Quad SPI setting, Security Register lock status, and Erase / Program Suspend status.

SR1 and SR2 contain non-volatile bits in locations SR1[7:2] and SR2[6:0] that control sector protection, OTP Register Protection, Status Register Protection, and Quad mode. Bits located in SR2[7], SR1[1], and

SR1[0] are read only volatile bits for suspend, write enable, and busy status. These are updated by the memory control logic. The SR1[1] write enable bit is set only by the Write Enable (06h) command and cleared by the memory control logic when an embedded operation is completed.

Write access to the non-volatile Status Register bits is controlled by the state of the non-volatile Status Register Protect bits SR1[7] and SR2[0] (SRP0, SRP1), the Write Enable command (06h) preceding a Write Status Registers command, and while Quad mode is not enabled, the WP# pin.

A volatile version of bits SR2[6], SR2[1], and SR1[7:2] that control sector protection and Quad Mode is used to control the behavior of these features after power up. During power up or software reset, these volatile bits are loaded from the non-volatile version of the Status Register bits. The Write Enable for Volatile Status Register (50h) command can be used to write these volatile bits when the command is followed by a Write Status Registers (01h/31h) command. This gives more flexibility to change the system configuration and memory protection schemes quickly without waiting for the typical non-volatile bit write cycles or affecting the endurance of the Status Register non-volatile bits.

Write access to the volatile SR1 and SR2 Status Register bits is controlled by the state of the non-volatile Status Register Protect bits SR1[7] and SR2[0] (SRP0, SRP1), the Write Enable for Volatile Status Register command (50h) preceding a Write Status Registers command, and the WP# pin while Quad mode is not enabled.

Status Register-3 (SR3) is used to configure and provide status on the variable HOLD# or RESET# function, Output Driver Strength, High Frequency Enable Bit and read latency.

Write access to the volatile SR3 Status Register bits is controlled by Write Enable for Volatile Status Register command (50h) preceding a Write Status Register command. The SRP bits do not protect SR3.

Table 6.1 Status Register-1 (SR1)

Bits	Field	Function	Type	Default State	Description
7	SRP0	Status Register Protect 0	Non-volatile and Volatile versions	0	0 = WP# input has no effect or Power Supply Lock Down mode 1 = WP# input can protect the Status Register or OTP Lock Down.
6	SEC	Sector / Block Protect		0	0 = BP2-BP0 protect 64-kB blocks 1 = BP2-BP0 protect 4-kB sectors
5	TB	Top / Bottom protect		0	0 = BP2-BP0 protect from the Top down 1 = BP2-BP0 protect from the Bottom up
4	BP2	Block Protect Bits		0	000b = No protection
3	BP1			0	
2	BP0		0		
1	WEL	Write Enable Latch	Volatile, Read only	0	0 = Not Write Enabled, no embedded operation can start 1 = Write Enabled, embedded operation can start
0	BUSY	Embedded Operation Status	Volatile, Read only	0	0 = Not Busy, no embedded operation in progress 1 = Busy, embedded operation in progress

Table 6.2 Status Register-2 (SR2)

Bits	Field	Function	Type	Default State	Description
7	SUS	Suspend Status	Volatile, Read Only	0	0 = Erase / Program not suspended 1 = Erase / Program suspended
6	CMP	Complement Protect	Non-volatile and Volatile versions	0	0 = Normal Protection Map 1 = Complementary Protection Map
5	LB3	Security Register Lock Bits	OTP	0	OTP Lock Bits 3:0 for Security Registers 3:0 0 = Security Register not protected 1 = Security Register protected
4	LB2			0	
3	LB1			0	
2	Reserve			0	
1	QE	Quad Enable	Non-volatile and Volatile versions	0	0 = Quad Mode Not Enabled, the WP# pin and HOLD# / RESET# are enabled 1 = Quad Mode Enabled, the IO2 and IO3 pins are enabled, and WP# and HOLD# / RESET# functions are disabled
0	SRP1	Status Register Protect 1		0	0 = SRP1 selects whether WP# input has effect on protection of the status register 1 = SRP1 selects Power Supply Lock Down or OTP Lock Down mode

Table 6.3 Status Register-3 (SR3)

Bits	Field	Function	Type	Default State	Description
7	HRSW ⁽¹⁾	HOLD# or RESET# function	Non-volatile and Volatile versions	0	When HRSW=0, the pin acts as HOLD#; when HRSW=1, the pin acts as RESET#. HRSW functions are only available when QE=0.
6	DRV1 ⁽¹⁾	Output Driver Strength	Volatile	0	The DRV1 & DRV0 bits are used to determine the output driver strength for the Read operations.
5	DRV0 ⁽¹⁾			0	
4	HFM	High Frequency Mode Enable Bit	Non-volatile and Volatile versions	0	0 =High Frequency Mode Disabled 1 =High Frequency Mode Enabled
3	Reserve			0	
2				0	
1				0	
0				0	

Note:

1.Default state for these three bits could be modified. please contact sales.

6.2.1 BUSY

BUSY is a read only bit in the status register (SR1[0]) which is set to a “1” state when the device is executing a Page Program, Sector Erase, Block Erase, Chip Erase or Write Status Register instruction. During this time the device will ignore further instructions except for the Read Status Register instruction (see t_w , t_{pp} , t_{se} , t_{be} , and t_{ce} in AC Characteristics). When the program, erase or write status register instruction has completed, the BUSY bit will be cleared to a “0” state indicating the device is ready for further instructions.

6.2.2 Write Enable Latch (WEL)

Write Enable Latch (WEL) is a read only bit in the status register (SR1[1]) which is set to a 1 after executing a Write Enable Instruction. The WEL status bit is cleared to a 0 when the device is written disabled. A write disable state occurs upon power-up or after any of the following instructions: Write Disable, Page Program, Sector Erase, Block Erase, Chip Erase and Write Status Register.

6.2.3 Block Protect Bits (BP2, BP1, BP0)

The Block Protect Bits (BP2, BP1, BP0) are non-volatile read / write bits in the Status Register (SR1[4:2]) that provide Write Protection control and status. Block Protect bits can be set using the Write Status Registers Command (see t_w in Section 8.5). All, none or a portion of the memory array can be protected from Program and Erase commands (see Section 6.4.2, Block Protection Maps). The factory default setting for the Block Protection Bits is 0 (none of the array is protected.)

6.2.4 Top / Bottom Block Protect (TB)

The non-volatile Top / Bottom bit (TB SR1[5]) controls whether the Block Protect Bits (BP2, BP1, BP0) protect from the Top (TB=0) or the Bottom (TB=1) of the array as shown in Section 6.4.2, Block Protection Maps. The factory default setting is TB=0. The TB bit can be set with the Write Status Registers Command depending on the state of the SRP0, SRP1 and WEL bits.

6.2.5 Sector / Block Protect (SEC)

The non-volatile Sector / Block Protect bit (SEC SR1[6]) controls if the Block Protect Bits (BP2, BP1, BP0) protect either 4-kB Sectors (SEC=1) or 64-kB Blocks (SEC=0) of the array as shown in Section 6.4.2, Block

Protection Maps. The default setting is SEC=0.

6.2.6 Complement Protect (CMP)

The Complement Protect bit (CMP SR2[6]) is a non-volatile read / write bit in the Status Register (SR2[6]). It is used in conjunction with SEC, TB, BP2, BP1 and BP0 bits to provide more flexibility for the array protection. Once CMP is set to 1, previous array protection set by SEC, TB, BP2, BP1 and BP0 will be reversed. For instance, when CMP=0, a top 4-kB sector can be protected while the rest of the array is not; when CMP=1, the top 4-kB sector will become unprotected while the rest of the array become read-only. Refer to Section 6.4.2, Block Protection Maps for details. The default setting is CMP=0.

6.2.7 The Status Register Protect (SRP1, SRP0)

The Status Register Protect bits (SRP1 and SRP0) are non-volatile read / write bits in the Status Register (SR2[0] and SR1[7]). The SRP bits control the method of write protection: software protection, hardware protection, power supply lock-down, or one time programmable (OTP) protection.

Table 6.4 Status Register Protect

SRP1	SRP0	WP#	Status Register	Description
0	0	X	Software Protection	WP# pin has no control. SR1 and SR2 can be written to after a Write Enable command, WEL=1. [Factory Default]
0	1	0	Hardware Protected	When WP# pin is low the SR1 and SR2 are locked and cannot be written.
0	1	1	Hardware Unprotected	When WP# pin is high SR1 and SR2 are unlocked and can be written to after a Write Enable command, WEL=1.
1	0	X	Power Supply Lock Down	SR1 and SR2 are protected and cannot be written to again until the next power-down, power-up cycle. ⁽¹⁾
1	1	X	One Time Program ⁽²⁾	SR1 and SR2 are permanently protected and cannot be written.

Notes:

- When SRP1, SRP0 = (1, 0), a power-down, power-up, or Software Reset cycle will change SRP1, SRP0 to (0, 0) state.
- The One-Time Program feature is available upon special order. Contact Zbit for details.
- Busy, WEL, and SUS (SR1[1:0] and SR2[7]) are volatile read only status bits that are never affected by the Write Status Registers command.
- The non-volatile version of HRSW, HFM, CMP, QE, SRP1, SRP0, SEC, TB, and BP2-BP0 (SR3[7,4], SR2[6,1,0] and SR1[6:2]) bits and the OTP LB3-LB1 bits are not writable when protected by the SRP bits and WP# as shown in the table. The non-volatile version of these Status Register bits is selected for writing when the Write Enable (06h) command precedes the Write Status Registers (01h) command.
- The volatile version of HRSW, DRV1, DRV0, HFM, CMP, QE, SRP1, SRP0, SEC, TB, and BP2-BP0 (SR3[7:4], SR2[6,1,0] and SR1[6:2]) bits are not writable when protected by the SRP bits and WP# as shown in the table. The volatile version of these Status Register bits is selected for writing when the Write Enable for volatile Status Register (50h) command precedes the Write Status Registers (01h) command. There is no volatile version of the LB3-LB1 bits and these bits are not affected by a volatile Write Status Registers command.

6.2.8 Erase / Program Suspend Status (SUS)

The Suspend Status bit is a read only bit in the status register (SR2[7]) that is set to 1 after executing an Erase / Program Suspend (75h) command. The SUS status bit is cleared to 0 by Erase / Program Resume (7Ah) command as well as a power-down, power-up cycle.

6.2.9 Security Register Lock Bits (LB3, LB2, LB1)

The Security Register Lock Bits (LB3, LB2, LB1) are non-volatile One Time Program (OTP) bits in Status Register (SR2[5:2]) that provide the write protect control and status to the Security Registers. The default state of LB[3:1] is 0, Security Registers 1 to 3 are unlocked. LB[3:1] can be set to 1 individually using the Write Status Registers command. LB[3:1] are One Time Programmable (OTP), once it's set to 1, the corresponding 256-byte Security Register will become read-only permanently.

6.2.10 Quad Enable (QE)

The Quad Enable (QE) bit is a non-volatile read / write bit in the Status Register (SR2[1]) that allows

Quad SPI operation. When the QE bit is set to a 0 state (factory default), the WP# pin and HOLD# / RESET# are enabled. When the QE bit is set to a 1, the Quad IO2 and IO3 pins are enabled, and WP# and HOLD# / RESET# functions are disabled.

Note: If the WP# or HOLD# / RESET# pins are tied directly to the power supply or ground during standard SPI or Dual SPI operation, the QE bit should never be set to a 1.

6.2.11 HOLD# or RESET# Pin Function (HRSW)

The HRSW bit is used to determine whether HOLD# or RESET# function should be implemented on the hardware pin for 8-pin packages. When HRSW=0, the pin acts as #HOLD; when HRSW=1, the pin acts as RESET#. However, HOLD# or RESET# functions are only available when QE=0. If QE is set to 1, the HOLD# and RESET# functions are disabled, the pin acts as a dedicated data I/O pin.

6.2.12 Output Driver Strength (DRV1, DRV0)

The DRV1 & DRV0 bits are used to determine the output driver strength for the Read operations.

DRV1, DRV0	Driver Strength
0, 0	50%
0, 1	25%
1, 0	75%(default)
1, 1	100%

6.2.13 High Frequency Mode Enable Bit (HFM)

The HFM bit is used to determine whether the device is in High Frequency Mode. When HFM bit sets to 1, it means the device is in High Frequency Mode, when HFM bit sets 0 (default), it means the device is not in High Frequency Mode. This Mode allows pre-charge of internal charge pump, so the voltages required for accessing the flash memory array are readily available for read. After the HFM is executed, the device will maintain a slightly higher standby current (ICC8) than standard SPI operation.

6.3. Write Protection

Applications that use non-volatile memory must take into consideration the possibility of noise and other adverse system conditions that may compromise data integrity. To address this concern the ZB25VQ80 provides the following data protection mechanisms:

6.3.1 Write Protect Features

- ◆ Device resets when V_{CC} is below threshold
- ◆ Time delay write disable after Power-Up
- ◆ Write enable / disable commands and automatic write disable after erase or program
- ◆ Command length protection
 - All commands that Write, Program or Erase must complete on a byte boundary (CS# driven high after a full 8 bits have been clocked) otherwise the command will be ignored.
- ◆ Software and Hardware write protection using Status Register control
 - WP# input protection
 - Lock Down write protection until next power-up or Software Reset
 - One-Time Program (OTP) write protection
- ◆ Write Protection using the Deep Power-Down command

Upon power-up or at power-down, the ZB25VQ80 will maintain a reset condition while V_{CC} is below the threshold value of VWI, (see Figure 8.1). While reset, all operations are disabled and no commands are recognized. During power-up and after the V_{CC} voltage exceeds VWI, all program and erase related commands are further disabled for a time delay of tPUW. This includes the Write Enable, Page Program, Sector Erase, Block Erase, Chip Erase and the Write Status Registers commands. Note that the chip select pin (CS#) must track the V_{CC} supply level at power-up until the V_{CC} -min level and tVSL time delay is reached. If needed a pull-up resistor on CS# can be used to accomplish this.

After power-up the device is automatically placed in a write-disabled state with the Status Register Write Enable Latch (WEL) set to a 0. A Write Enable command must be issued before a Page Program, Sector Erase, Block Erase, Chip Erase or Write Status Registers command will be accepted. After completing a program, erase or write command the Write Enable Latch (WEL) is automatically cleared to a write-disabled state of 0.

Software controlled main flash array write protection is facilitated using the Write Status Registers command to write the Status Register (SR1,SR2) and Block Protect (SEC, TB, BP2, BP1 and BP0) bits.

The BP method allows a portion as small as 4-kB sector or the entire memory array to be configured as read only. Used in conjunction with the Write Protect (WP#) pin, changes to the Status Register can be enabled or disabled under hardware control. See the Table 6.4 for further information.

Additionally, the Deep Power-Down (DPD) command offers an alternative means of data protection as all commands are ignored during the DPD state, except for the Release from Deep-Power-Down (RES ABh) command. Thus, preventing any program or erase during the DPD state.

6.3.2 Block Protection Maps

Table 6.6 ZB25VQ80 Block Protection (CMP = 0)

Status Register ⁽¹⁾					ZB25VQ80(8 Mbit) Block Protection (CMP=0) ⁽²⁾			
SEC	TB	BP2	BP1	BP0	Protected Block(s)	Protected Addresses	Protected Density	Protected Portion
X	X	0	0	0	None	None	None	None
0	0	0	0	1	15	0F0000h – 0FFFFFFh	64 kB	Upper 1/16
0	0	0	1	0	14 and 15	0E0000h – 0FFFFFFh	128 kB	Upper 1/8
0	0	0	1	1	12 thru 15	0C0000h – 0FFFFFFh	256 kB	Upper 1/4
0	0	1	0	0	8 thru 15	080000h – 0FFFFFFh	512 kB	Upper 1/2
0	1	0	0	1	0	000000h – 00FFFFh	64 kB	Lower 1/16
0	1	0	1	0	0 and 1	000000h – 01FFFFh	128 kB	Lower 1/8
0	1	0	1	1	0 thru 3	000000h – 03FFFFh	256 kB	Lower 1/4
0	1	1	0	0	0 thru 7	000000h – 07FFFFh	512 kB	Lower 1/2
0	X	1	0	1	0 thru 15	000000h – 0FFFFFFh	1 MB	All
X	X	1	1	X	0 thru 15	000000h – 0FFFFFFh	1 MB	All
1	0	0	0	1	15	0FF000h – 0FFFFFFh	4 kB	Upper 1/256
1	0	0	1	0	15	0FE000h – 0FFFFFFh	8 kB	Upper 1/128
1	0	0	1	1	15	0FC000h – 0FFFFFFh	16 kB	Upper 1/64
1	0	1	0	X	15	0F8000h – 0FFFFFFh	32 kB	Upper 1/32
1	1	0	0	1	0	000000h – 000FFFh	4 kB	Lower 1/256
1	1	0	1	0	0	000000h – 001FFFh	8 kB	Lower 1/128
1	1	0	1	1	0	000000h – 003FFFh	16 kB	Lower 1/64
1	1	1	0	X	0	000000h – 007FFFh	32 kB	Lower 1/32

Notes:

1. X = don't care.
2. If any Erase or Program command specifies a memory region that contains protected data portion, this command will be ignored.

Table 6.7 ZB25VQ80 Block Protection (CMP = 1)

Status Register ⁽¹⁾					ZB25VQ80(8 Mbit) Block Protection (CMP=1) ⁽²⁾			
SEC	TB	BP2	BP1	BP0	Protected Block(s)	Protected Addresses	Protected Density	Protected Portion
X	X	0	0	0	0 thru 15	000000h – 0FFFFFFh	1 MB	All
0	0	0	0	1	0 thru 14	000000h – 0EFFFFh	960 kB	Lower 15/16
0	0	0	1	0	0 thru 13	000000h – 0DFFFFh	896 kB	Lower 7/8
0	0	0	1	1	0 thru 11	000000h – 0BFFFFh	768 kB	Lower 3/4
0	0	1	0	0	0 thru 7	000000h – 07FFFFh	512 kB	Lower 1/2
0	1	0	0	1	1 thru 15	010000h – 0FFFFFFh	960 kB	Upper 15/16
0	1	0	1	0	2 thru 15	020000h – 0FFFFFFh	896 kB	Upper 7/8
0	1	0	1	1	4 thru 15	040000h – 0FFFFFFh	768 kB	Upper 3/4
0	1	1	0	0	8 thru 15	080000h – 0FFFFFFh	512 kB	Upper 1/2
0	X	1	0	1	None	None	None	None
X	X	1	1	X	None	None	None	None
1	0	0	0	1	0 thru 15	000000h – 0FEFFFFh	1020 kB	Lower 255/256
1	0	0	1	0	0 thru 15	000000h – 0FDFFFFh	1016 kB	Lower 127/128
1	0	0	1	1	0 thru 15	000000h – 0FBFFFFh	1008 kB	Lower 63/64
1	0	1	0	X	0 thru 15	000000h – 0F7FFFFh	992 kB	Lower 31/32
1	1	0	0	1	0 thru 15	001000h – 0FFFFFFh	1020 kB	Upper 255/256
1	1	0	1	0	0 thru 15	002000h – 0FFFFFFh	1016 kB	Upper 127/128
1	1	0	1	1	0 thru 15	004000h – 0FFFFFFh	1008 kB	Upper 63/64
1	1	1	0	X	0 thru 15	008000h – 0FFFFFFh	992 kB	Upper 31/32

Notes:

1. X = don't care.
2. If any Erase or Program command specifies a memory region that contains protected data portion, this command will be ignored.

6.4. Page Program

To program one data byte, two instructions are required: Write Enable (WREN), which is one byte, and a Page Program (PP) sequence, which consists of four bytes plus data. This is followed by the internal Program cycle (of duration t_{PP}). To spread this overhead, the Page Program (PP) instruction allows up to 256 bytes to be programmed at a time (changing bits from 1 to 0), provided that they lie in consecutive addresses on the same page of memory.

6.5. Sector Erase, Block Erase and Chip Erase

The Page Program (PP) instruction allows bits to be reset from 1 to 0. Before this can be applied, the bytes of memory need to be erased to all 1s (FFh). This can be achieved a sector at a time, using the Sector Erase (SE) instruction, a block at a time using the Block Erase (BE) instruction or throughout the entire memory, using the Chip Erase (CE) instruction. This starts an internal Erase cycle (of duration t_{SE} , t_{BE} or t_{CE}). The Erase instruction must be preceded by a Write Enable (WREN) instruction.

6.6. Polling during a Write, Program or Erase Cycle

A further improvement in the time to Write Status Register (WRSR), Program (PP) or Erase (SE, BE or CE) can be achieved by not waiting for the worst case delay (t_W , t_{PP} , t_{SE} , t_{BE} or t_{CE}). The Write In Progress (WIP) bit is provided in the Status Register so that the application program can monitor its value, polling it to establish when the previous Write cycle, Program cycle or Erase cycle is complete.

6.7. Active Power, Stand-by Power and Deep Power-Down Modes

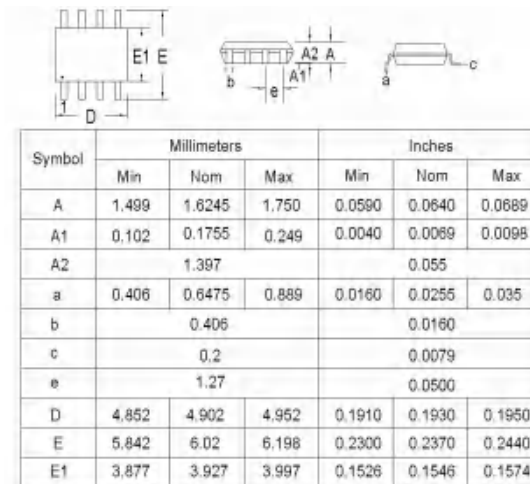
When Chip Select (CS#) is Low, the device is enabled, and in the Active Power mode. When Chip Select (CS#) is High, the device is disabled, but could remain in the Active Power mode until all internal cycles have completed (Program, Erase, Write Status Register). The device then goes into the Standby Power mode. The device consumption drops to ICC1.

The Deep Power-down mode is entered when the specific instruction (the Enter Deep Power-down Mode (DP) instruction) is executed. The device consumption drops further to ICC2. The device remains in this mode until another specific instruction (the Release from Deep Power-down Mode and Read Device ID (RDI) instruction) is executed.

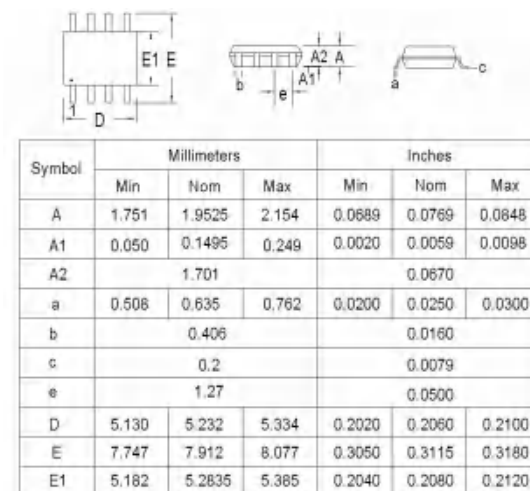
All other instructions are ignored while the device is in the Deep Power-down mode. This can be used as an extra software protection mechanism, when the device is not in active use, to protect the device from inadvertent Program or Erase instructions.

9. PACKAGE MECHANICAL

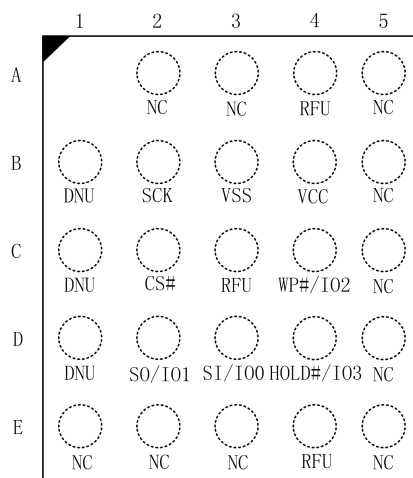
9.1. 8-Pin SOIC 150-mil



9.2. 8-Pin SOIC 208-mil



9.5. FAB024 24-Ball BGA



9.6. FAC024 24-Ball BGA Package

