300mA,Ultra-low noise, Small Package Ultra-Fast CMOS LDO Regulator

General Description

The LP3980 is designed for portable RF and wireless applications demanding performance and space requirements. The LP3980 performance is optimized for battery-powered systems to deliver ultra low noise and low quiescent current. Regulator ground current increases only slightly in dropout, further prolonging the battery life. The LP3980 also works with low-ESR ceramic capacitors, reducing the amount of board space necessary for power applications, critical in hand-held wireless devices. The LP3980 consumes less than 0.01μA in shutdown mode and has fast turn-on time less than 50μs. The other features include ultra low dropout voltage, high output accuracy, current limiting protection, and high ripple rejection ratio.

Applications

- ✧ Portable Media Players/MP3 players
- ✧ Cellular and Smart mobile phone
- ✧ LCD
- ✧ DSC Sensor
- ✧ Wireless Card

Features

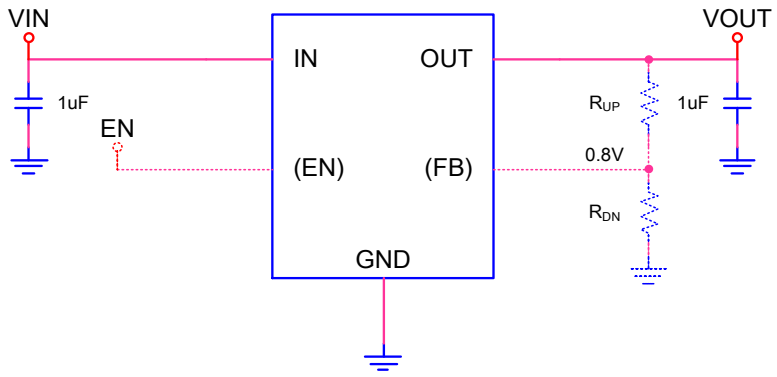
- ◆ 1.6V- 5.5V Input Voltage Range
- ◆ Low Dropout : 240mV @ 300mA,3.3V
- ◆ 300mA Output Current
- ◆ High PSRR: -76dB at 1KHz
- ◆ < 1μA Standby Current When Shutdown
- ◆ Ultra-Fast Response in Line/Load transient
- ◆ Current Limiting
- ◆ Thermal Shutdown Protection
- ◆ Available in SOT23-5/SOT23/TDFN-4 Package

Order Information

LP3980 □□ □□ □

- F: Pb-Free
- Package Type
  - B5 : SOT23-5
  - B3 : SOT23
  - QV: TDFN-4(1*1)
- Output Voltage Type
  - 11 : 1.1V
  - 12 : 1.2V
  - 15 : 1.5V
  - 18 : 1.8V
  - 25 : 2.5V
  - 28 : 2.8V
  - 30 : 3.0V
  - 33 : 3.3V
  - 50 : 5.0V
  - A : ADJ

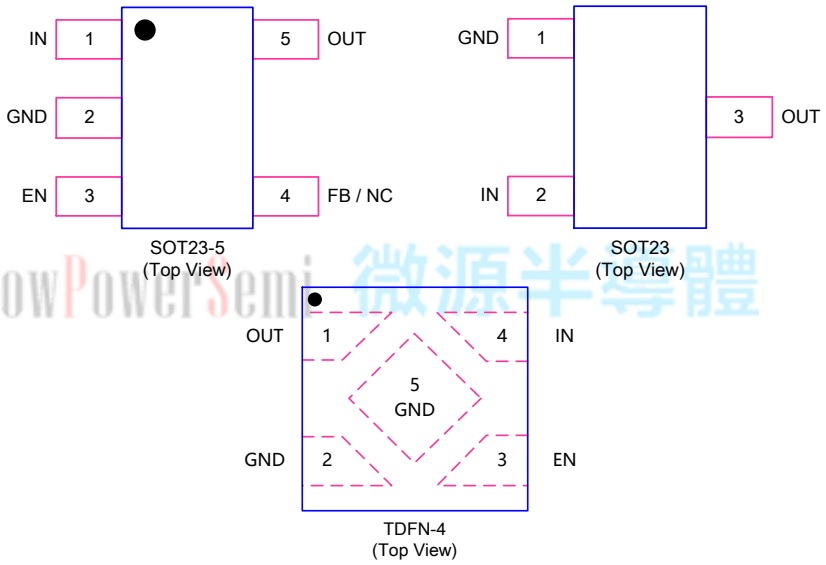
Typical Application Circuit



Note1: Only the SOT23-5/TDFN-4 package has an EN pin.

Note2: Only LP3980AB5F has an FB pin. The reference voltage is 0.8V. $V_{OUT} = 0.8V \times \left(1 + \frac{R_{UP}}{R_{DN}}\right)$

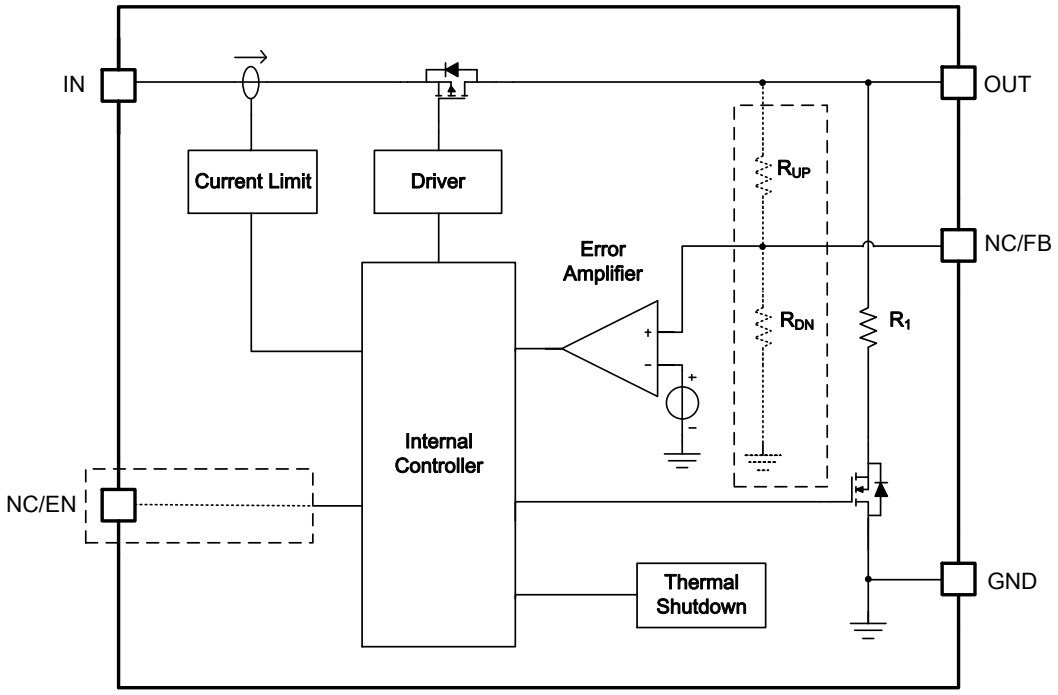
Functional Pin Description

Package Type	Pin Configurations
SOT23-5 SOT23 TDFN-4(1*1)	

Pin Description

Pin No.			Name	Description
SOT23-5	SOT23	TDFN-4		
1	2	4	VIN	Power Input voltage.
2	1	2	GND	Ground.
3	-	3	EN	Enable pin.
4	-	-	NC	No connect.
			FB (LP3980A)	Feedback pin. The reference voltage is 0.8V.
5	3	1	OUT	Output voltage.

Functional Block Diagram



Absolute Maximum Ratings Note 1

- ✧ Input to GND ---------- -0.3V to 6V
- ✧ EN to GND ---------- -0.3V to 6V
- ✧ Output Voltage to GND ---------- -0.3V to (V_{IN}+0.3V)
- ✧ Maximum Junction Temperature (T_J) ---------- 150℃
- ✧ Operating Ambient Temperature Range (T_A) ---------- -40℃ to 85℃
- ✧ Maximum Soldering Temperature (At leads, 10 sec) ---------- 260℃

Note 1. Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Thermal Information

- ✧ Maximum Power Dissipation (SOT23-5, P_D, T_A=25℃) ---------- 400mW
- ✧ Thermal Resistance (SOT23-5, θ_{JA}) ---------- 250℃/W
- ✧ Maximum Power Dissipation (SOT23, P_D, T_A=25℃) ---------- 350mW
- ✧ Thermal Resistance (SOT23, θ_{JA}) ---------- 350℃/W
- ✧ Maximum Power Dissipation (TDFN-4, P_D, T_A=25℃) ---------- 390mW
- ✧ Thermal Resistance (TDFN-4, θ_{JA}) ---------- 256℃/W

ESD Susceptibility

- ✧ HBM(Human Body Model) ---------- 2KV
- ✧ MM(Machine Model) ---------- 200V

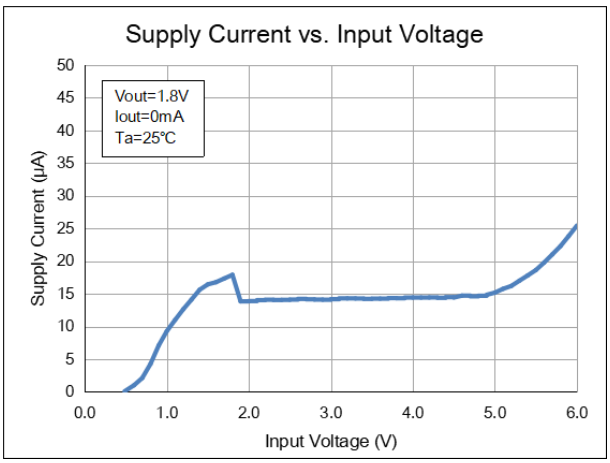
Electrical Characteristics

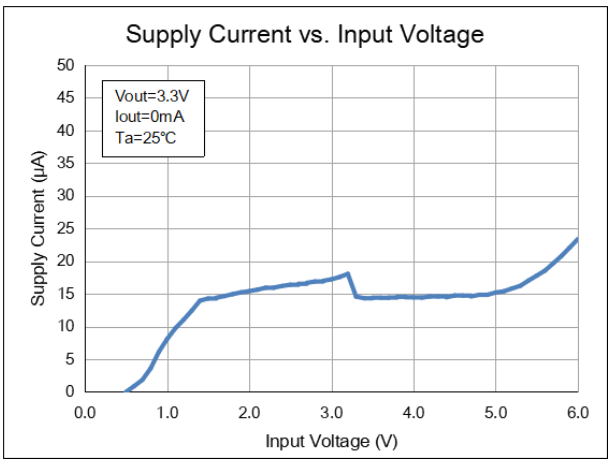
(V_{IN}=V_{OUT} + 1V, C_{IN}=C_{OUT}=1μF , T_A=25℃, unless otherwise specified.)

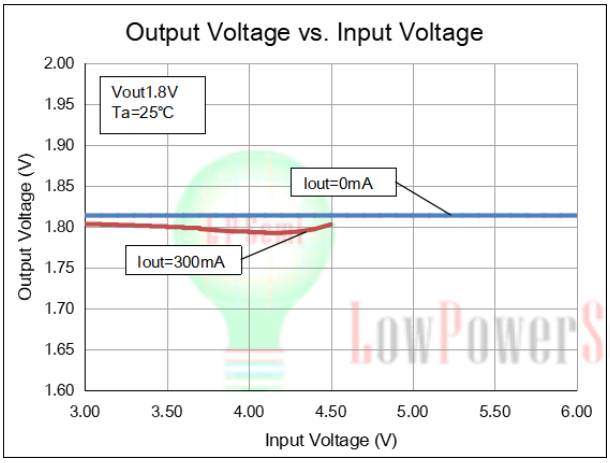
Parameter		Symbol	Test Conditions	Min	Typ.	Max	Units
Input Voltage		V_{IN}		1.6		5.5	V
Output Voltage Accuracy		ΔV_{OUT}	I_{OUT}=1mA	−2		+2	%
Feedback Voltage		V_{FB}	LP3980AB5F, I_{OUT}=1mA	0.784	0.800	0.816	V
Maximum Output Current		I_{max}	V_{EN}=V_{IN}>2.5V		300		mA
Current Limit		I_{LIM}	R_{LOAD}=1Ω		650		mA
Quiescent Current		I_Q	V_{EN}>1.2V, I_{OUT}=0mA		20		μA
Dropout Voltage		V_{DROP}	I_{OUT}=300mA, V_{OUT}=1.2V		650		mV
			I_{OUT}=300mA, V_{OUT}=1.8V		360		mV
			I_{OUT}=300mA, V_{OUT}=2.8V		260		mV
			I_{OUT}=300mA, V_{OUT}=3.3V		240		mV
Line Regulation		$\frac{\Delta V_{OUT}}{\Delta V_{IN} \times V_{OUT}}$	V_{OUT}=1.2V, I_{OUT}=1mA, V_{IN}=2.2V to 5.5V			0.4	%
			V_{OUT}=1.8V, I_{OUT}=1mA, V_{IN}=2.8V to 5.5V			0.3	%
			V_{OUT}=2.8V, I_{OUT}=1mA, V_{IN}=3.8V to 5.5V			0.3	%
			V_{OUT}=3.3V, I_{OUT}=1mA, V_{IN}=4.3V to 5.5V			0.3	%
Load Regulation		$\frac{\Delta V_{OUT}}{V_{OUT}}$	V_{OUT}=1.2V, I_{OUT}=1mA to 300mA			2	%
			V_{OUT}=1.8V, I_{OUT}=1mA to 300mA			1.5	%
			V_{OUT}=2.8V, I_{OUT}=1mA to 300mA			1	%
			V_{OUT}=3.3V, I_{OUT}=1mA to 300mA			1	%
Standby Current		I_{STBY}	V_{EN}=0V, Shutdown		0.01	1	μA
EN Input Bias Current		I_{IBSD}	V_{EN}=0V		0.1	1	μA
			V_{EN}=V_{IN}		0.1	1	μA
EN Threshold	Logic-Low Voltage	V_{IL}	V_{IN}=3V to 5.5V, Shutdown			0.4	V
	Logic-High Voltage	V_{IH}	V_{IN}=3V to 5.5V, Start-Up	1.4			V
Output Noise Voltage		-	f=10Hz to 100kHz, I_{OUT}=0mA, V_{OUT}=2.8V		100		μVRMS
Power Supply Rejection Rate	f=217Hz	PSRR	C_{OUT}=1μF, I_{OUT}=50mA		−80		dB
	f=1KHz				−76		dB
Thermal Shutdown Temperature		T_{SD}			150		℃

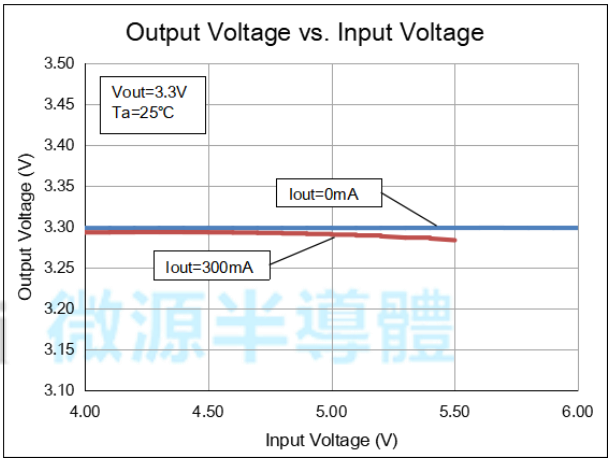
Typical Operating Characteristics

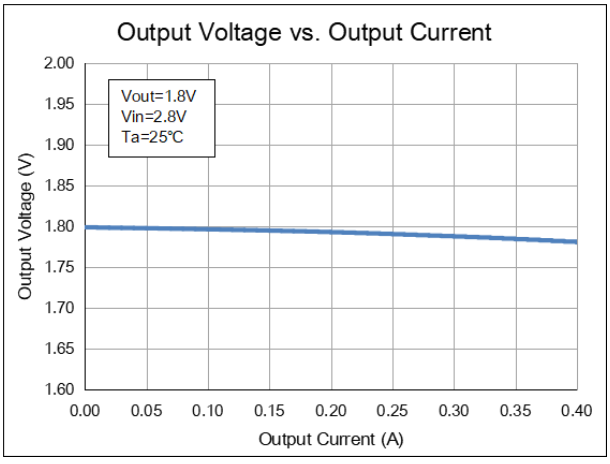
(C_{IN}=C_{OUT}=1uF, T_A=25℃, unless otherwise specified)

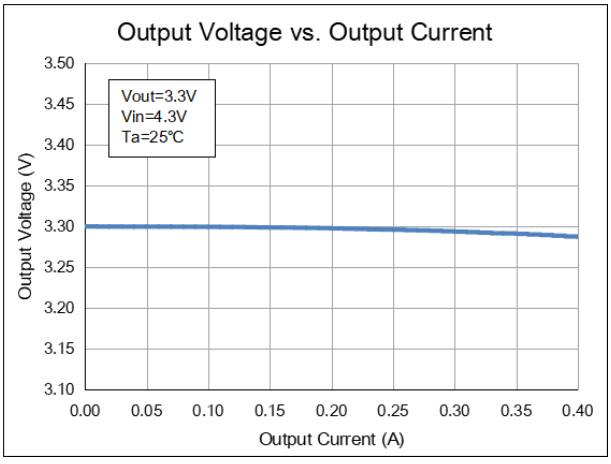






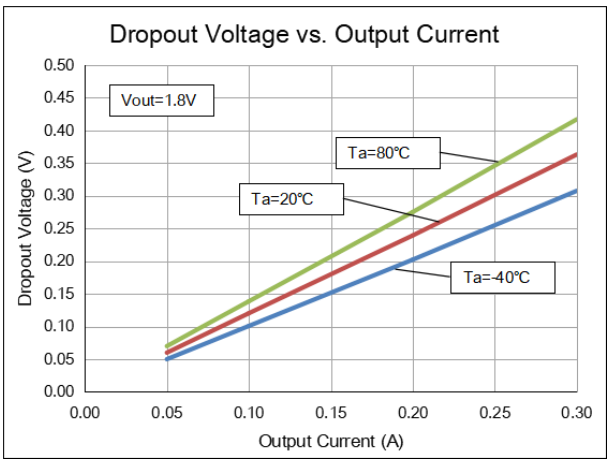


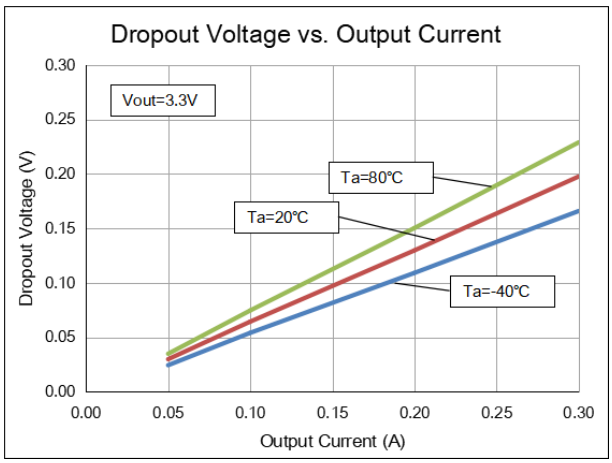


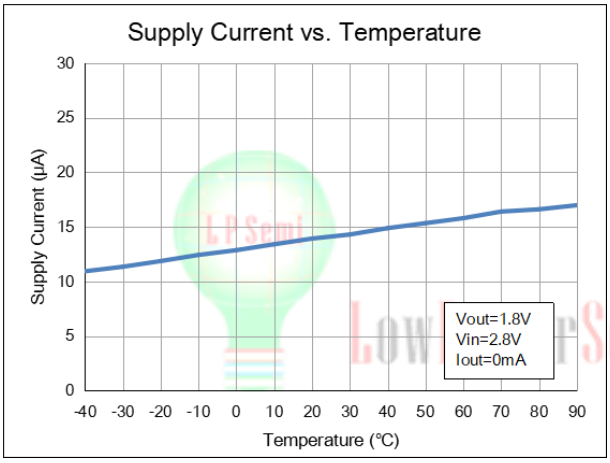


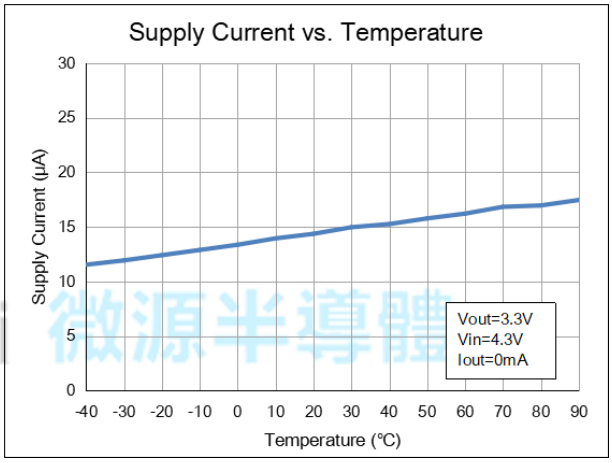
Typical Operating Characteristics

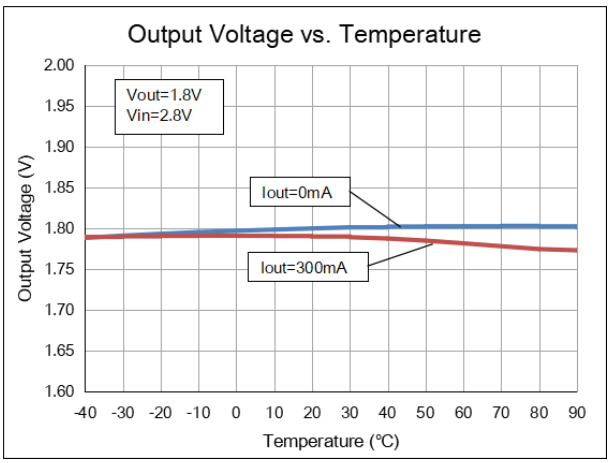
(C_{IN}=C_{OUT}=1uF, T_A=25℃, unless otherwise specified)

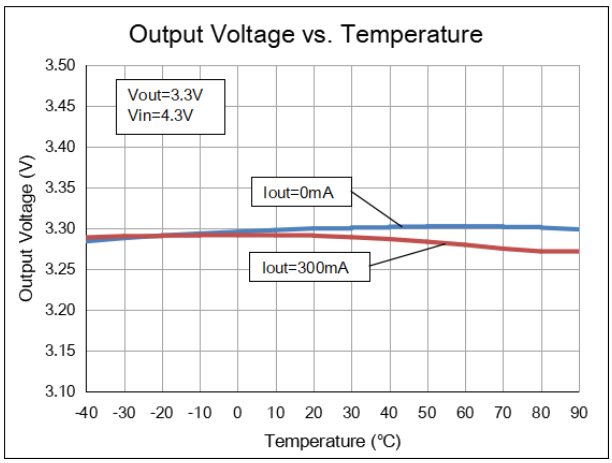






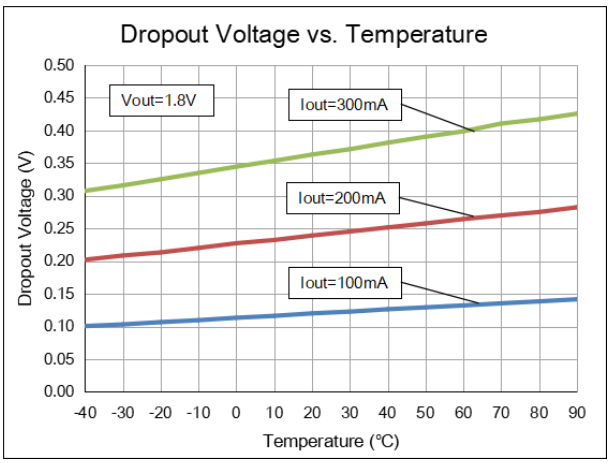


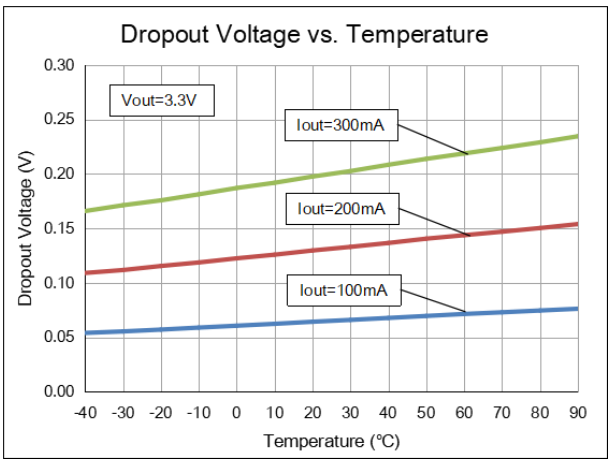


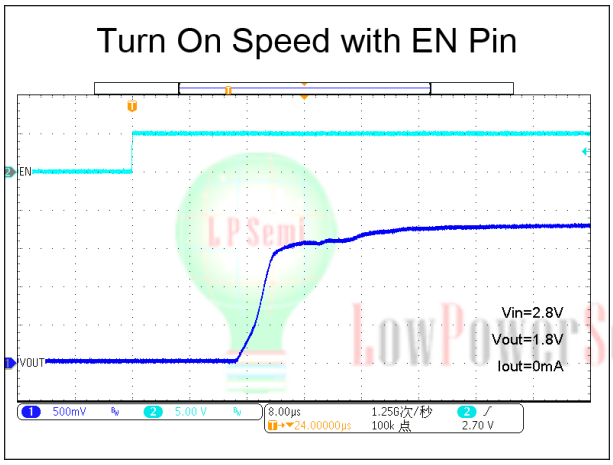


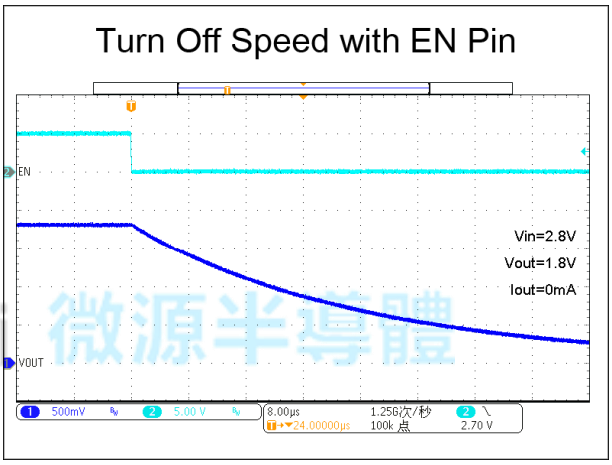
Typical Operating Characteristics

(C_{IN}=C_{OUT}=1uF, T_A=25℃, unless otherwise specified)









Applications Information

Like any low-dropout regulator, the external capacitors used with the LP3980 must be carefully selected for regulator stability and performance. Using a capacitor whose value is>1μF on the LP3980 input and the amount of capacitance can be increased without limit. The input capacitor must be located a distance of not more than 0.5 inch from the input pin of the IC and returned to a clean analog ground. Any good qμAlity ceramic or tantalum can be used for this capacitor. The capacitor with larger value and lower ESR (equivalent series resistance) provides better PSRR and line-transient response. The output capacitor must meet both requirements for minimum amount of capacitance and ESR in all LDOs application. The LP3980 is designed specifically to work with low ESR ceramic output capacitor in space-saving and performance consideration. Using a ceramic capacitor whose value is at least 1μF with ESR is>25mΩ on the LP3980 output ensures stability. The LP3980 still works well with output capacitor of other types due to the wide stable ESR range. Output capacitor of larger capacitance can reduce noise and improve load transient response, stability, and PSRR. The output capacitor should be located not more than 0.5 inch from the OUT pin of the LP3980 and returned to a clean analog ground.

Enable Function

The LP3980 features an LDO regulator enable/disable function. To assure the LDO regulator will switch on, the EN turn on control level must be greater than 1.4 volts. The LDO regulator will go into the shutdown mode when the voltage on the EN pin falls below 0.4 volts. For to protecting the system, the LP3980 have a quick-discharge function. If the enable function is not needed in a specific application, it may be tied to VIN to keep the LDO regulator in a continuously on state.

Thermal Considerations

Thermal protection limits power dissipation in LP3980. When the operation junction temperature exceeds 150℃, the OTP circuit starts the thermal shutdown function turn the pass element off. The pass element turns on again after the junction temperature cools by 20℃. For continue operation, do not exceed absolute maximum operation junction temperature 125℃.

The power dissipation definition in device is:

$$P_D = (V_{IN} - V_{OUT}) \times I_{OUT} + V_{IN} \times I_Q$$

The maximum power dissipation depends on the thermal resistance of IC package, PCB layout, the rate of surroundings airflow and temperature difference between junctions to ambient.

The maximum power dissipation can be calculated by following formula:

$$P_{D(MAX)} = \frac{(T_{J(MAX)} - T_A)}{\theta_{JA}}$$

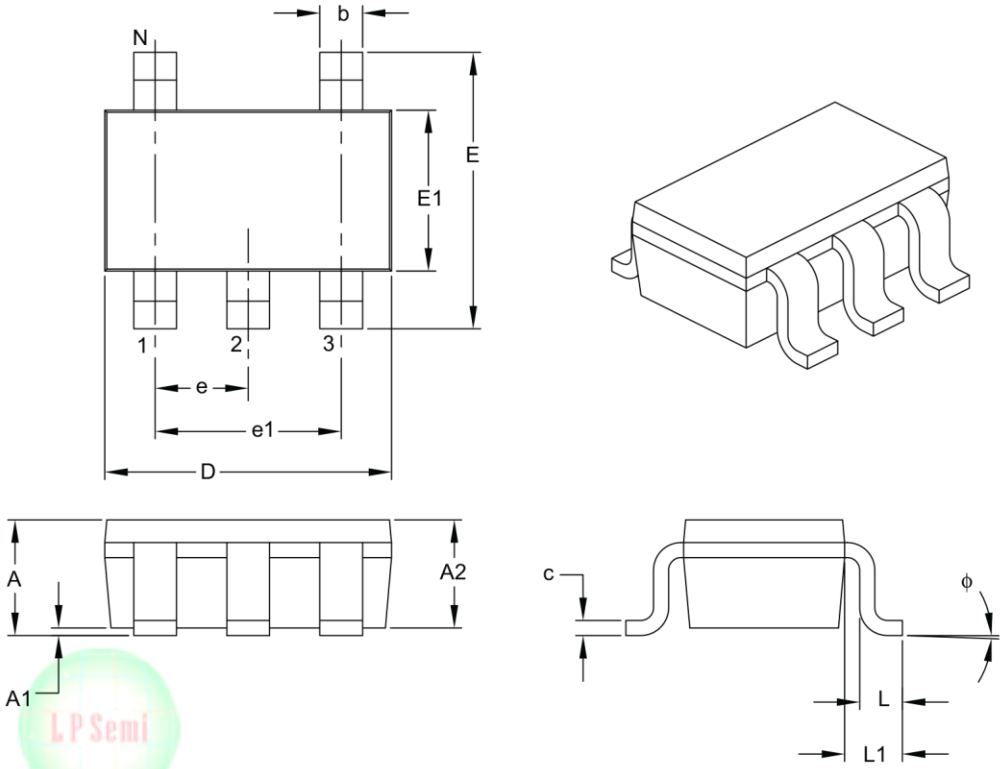
Where $T_{J(MAX)}$ is the maximum operation junction temperature 125℃, T_A is the ambient temperature and the θ_{JA} is the junction to ambient thermal resistance. For recommended operating conditions specification of LP3980, where $T_{J(MAX)}$ is the maximum junction temperature of the die (125℃) and T_A is the maximum ambient temperature. The junction to ambient thermal resistance (θ_{JA} is layout dependent) for SOT23-5 package is 250℃/W.

$$P_{D(MAX)} = \frac{(125℃ - 25℃)}{250℃/W} = 400mW$$

The maximum power dissipation depends on operating ambient temperature for fixed $T_{J(MAX)}$ and thermal resistance θ_{JA}.

Packaging Information

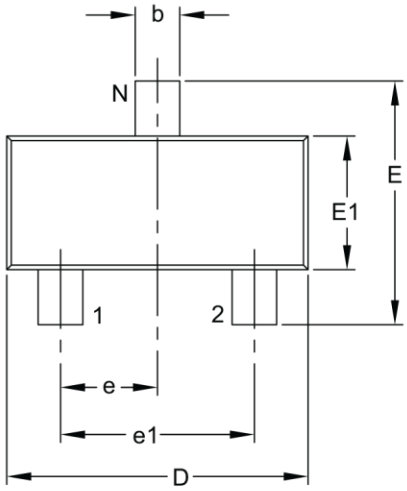
SOT23-5

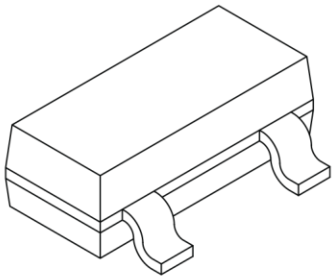


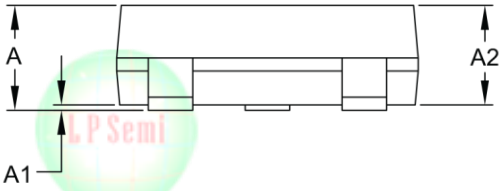
Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		5	
Lead Pitch	e		0.95 BSC	
Outside Lead Pitch	e1		1.90 BSC	
Overall Height	A	0.90	–	1.45
Molded Package Thickness	A2	0.89	–	1.30
Standoff	A1	0.00	–	0.15
Overall Width	E	2.20	–	3.20
Molded Package Width	E1	1.30	–	1.80
Overall Length	D	2.70	–	3.10
Foot Length	L	0.10	–	0.60
Footprint	L1	0.35	–	0.80
Foot Angle	ϕ	0°	–	30°
Lead Thickness	c	0.08	–	0.26
Lead Width	b	0.35	–	0.56

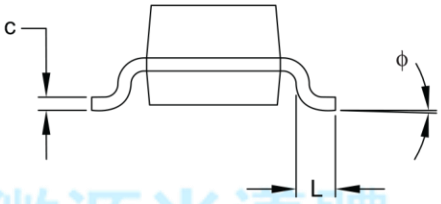
Packaging Information

SOT23





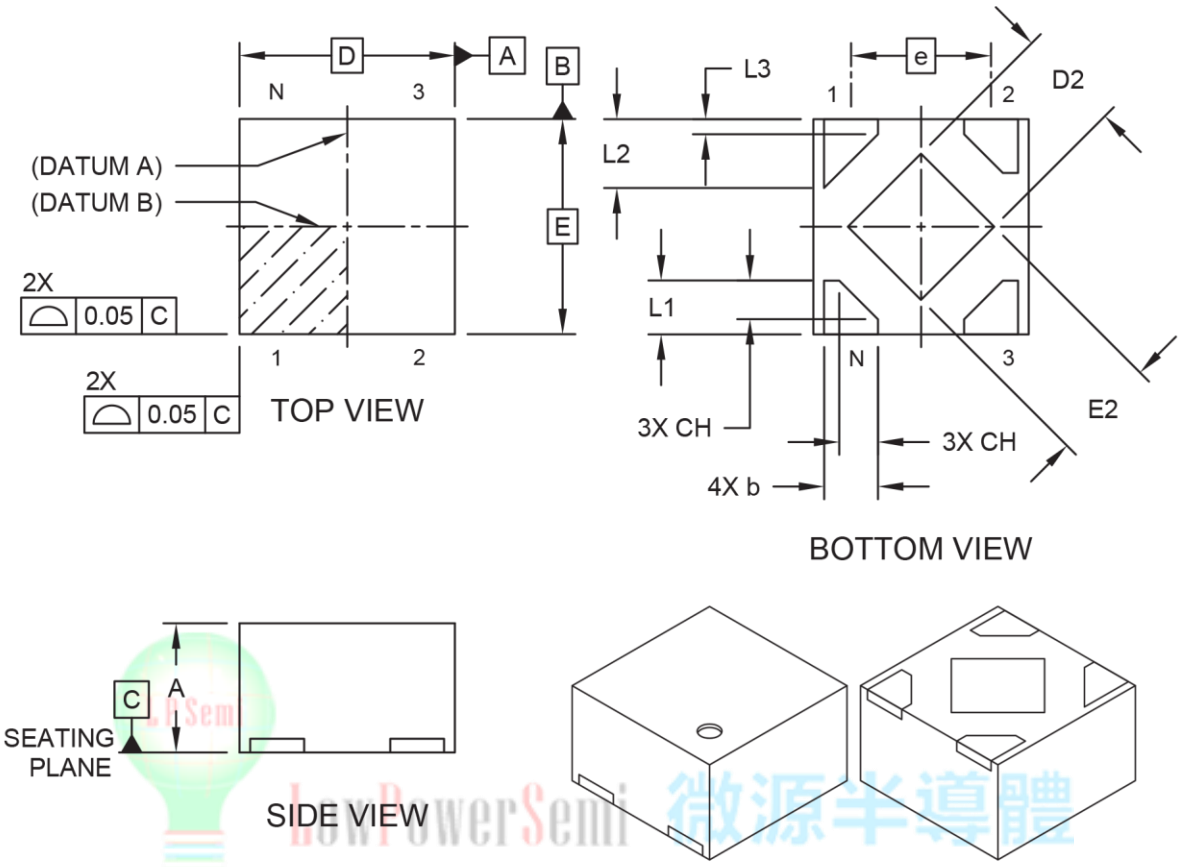




Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		3	
Lead Pitch	e		0.95 BSC	
Outside Lead Pitch	e1		1.90 BSC	
Overall Height	A	0.89	–	1.30
Molded Package Thickness	A2	0.79	0.95	1.02
Standoff	A1	0.01	–	0.10
Overall Width	E	2.59	–	3.00
Molded Package Width	E1	1.40	1.60	1.80
Overall Length	D	2.67	2.90	3.05
Foot Length	L	0.13	0.50	0.60
Foot Angle	ϕ	0°	–	10°
Lead Thickness	c	0.08	–	0.20
Lead Width	b	0.35	–	0.56

Packaging Information

TDFN-4



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Terminals	N		4	
Pitch	e		0.65 BSC	
Overall Height	A	-	-	0.60
Overall Width	E		1.00 BSC	
Exposed Pad Width	E2	0.43	0.48	0.53
Overall Length	D		1.00 BSC	
Exposed Pad Length	D2	0.43	0.48	0.53
Terminal Width	b	0.20	0.25	0.30
Terminal Length	L1	0.20	0.25	0.30
Terminal Length	L2	0.27	0.32	0.37
-	L3	0.02	0.07	0.12
Terminal Chamfer	CH	-	0.18	-